

Point Loma Nazarene University
CSC 454: Computer Architecture and Assembly Language
(4 units)
Fall 2016

Instructor:

Dr. Lori Carter, Professor of Computer Science
loricarter@pointloma.edu

(619) 849-2352
office: RS 214

Office hours:

M,W,F 10:30-12:00, 1:30-2:30

TR 1:30-2:30

Meeting Times and Location:

Lecture: M,W,F 8:30-9:35 RS 13

Lab: T 7:25-9:10 LW 220 (Bresee Lab)

Text:

Patterson and Hennessy, Computer Organization and Design. 5th edition. Morgan Kauffman.
Expect to cover most sections of chapters 1-6 along with Appendices A and B.

Catalog Description:

This course covers the fundamentals of current pipelined computer designs. Experience with assembly language programming and digital logic and circuit design will be used to motivate the need for certain facets of the more general instruction set architecture. Throughout the course, performance issues, hardware constraints, and memory hierarchy will be shown to inform processor design. Additional topics include integer and floating point arithmetic, I/O and considerations surrounding multi-core architectures. Lecture three hours and laboratory two hours each week.

Course Objectives:

- To provide an in-depth treatment of computer architecture, including digital logic, digital systems, computer pipelines, memory organization and processor design, both single and multi-core.
- To gain further understanding of computer organization and architecture by studying the MIPS assembly language and writing and analyzing programs using the SPIM simulator.
- To gain a better overall perspective of the interrelationship between computer architecture and other aspects of computer science including compilers, operating systems and programming.
- To gain an understanding of the tradeoffs considered when designing for increased performance including parallelism, power, convenience, and cost.

Course Learning Outcomes:

Students will analyze the interaction between hardware and software. Students will collaborate effectively in teams.

Course Organization:

Lectures: Cover the highlights of chapters assigned – not a substitute for reading. PowerPoint slides found on Canvas

Homework/ Homework quizzes: Homework will be assigned but not officially graded. Your homework grade will be based on a quiz administered on the day the homework is due. The quiz will cover concepts on the homework, but do not expect to do well on the quiz if you haven't actually worked through the homework. There will be **some** time for questions on the homework prior to taking the quiz, and you may look at your homework while taking the quiz. While **quizzes cannot be made up**, each student will be allowed to drop 1 homework quiz grade.

Expected quiz dates

Sept. 12	Sept. 19	Oct. 3	Oct. 12
Oct. 26	Nov. 9	Nov. 21	Dec. 2

Exams: There will be 2 exams. Exams will cover lecture as well as lab material. The first will cover chapters 1, 2 and Appendix A. The second will cover Appendix B and chapters 3 and 4. Students missing a midterm exam for a school function must arrange to take the exam in advance. Missed exams will likely result in a grade of 0. **Exams are currently scheduled for Sept. 27 and Nov. 11.**

Labs and Lab Projects: Labs will be demoed at the beginning (first 15 minutes) of the lab period in which they are due. Late labs are not accepted, but partial credit is awarded. Students may work alone, or in groups of 2 on the labs. If I suspect collaboration beyond a group of 2, interviews will be conducted and a grade of zero is possible for all collaborators. The grading method for each lab will be discussed when the lab is assigned. Students who are unable to answer questions about labs on their exams will be required to complete labs individually in the future.

Final Exam: Cumulative exam covering lecture and lab material. The Final exam is scheduled for **Monday, December 12, at 7:30 A.M.**

Grading:

Homework/Quizzes	15%	Exams	30%
Labs	30%	Final Exam	25%

Final grades will be determined as follows:

100-93%	A	80-82%	B-	67-69%	D+
90-92%	A-	77-79%	C+	63-66%	D
87-89%	B+	73-76%	C	60-62%	D-
83-86%	B	70-72%	C-	0-59%	F

Credit Hour Information:

In the interest of providing sufficient time to accomplish the stated course learning outcomes, this class meets the PLNU credit hour policy for a 4 unit class delivered over 15 weeks.

It is anticipated that you will spend a minimum of 37.5 participation hours per credit hour in your course. The estimated time expectations for this course are shown below:

Assignments	Total Course Hours
Reading	30
Written Homework	25
Lectures	40
Labs and Lab assignments	45
Exams and Quizzes	10
TOTAL	150 (for 4 course units)

University Mission:

Point Loma Nazarene University exists to provide higher education in a vital Christian community where minds are engaged and challenged, character is modeled and formed, and service is an expression of faith. Being of Wesleyan heritage, we strive to be a learning community where grace is foundational, truth is pursued, and holiness is a way of life.

MICS Department Mission:

The Mathematical, Information, and Computer Sciences department at Point Loma Nazarene University is committed to maintaining a curriculum that provides its students with the tools to be productive, the passion to continue learning, and Christian perspectives to provide a basis for making sound value judgments.

Attendance:

Attendance is expected at each class session. In the event of an absence you are responsible for the material covered in class and the assignments given that day.

Regular and punctual attendance at all classes is considered essential to optimum academic achievement. If the student is absent from more than 10 percent of class meetings, the faculty member can file a written report which may result in de-enrollment. If the absences exceed 20 percent, the student may be de-enrolled without notice until the university drop date or, after that date, receive the appropriate grade for their work and participation.

See [http://catalog.pointloma.edu/content.php?catoid=24&navoid=1581#Class Attendance](http://catalog.pointloma.edu/content.php?catoid=24&navoid=1581#Class_Attendance) in the Undergraduate Academic Catalog.

Class Enrollment:

It is the student's responsibility to maintain his/her class schedule. Should the need arise to drop this course (personal emergencies, poor performance, etc.), the student has the responsibility to follow through (provided the drop date meets the stated calendar deadline established by the university), not the instructor. Simply ceasing to attend this course or failing to follow through to arrange for a change of registration (drop/add) may easily result in a grade of F on the official transcript.

Academic Accommodations:

If you have a diagnosed disability, please contact PLNU's Disability Resource Center (DRC) within the first two weeks of class to demonstrate need and to register for accommodation by phone at 619-849-2486 or by e-mail at DRC@pointloma.edu. See [Disability Resource Center](#) for additional information. For more details

see the PLNU

catalog: http://catalog.pointloma.edu/content.php?catoid=24&navoid=1581#Academic_Accommodations

Students with learning disabilities who may need accommodations should discuss options with the instructor during the first two weeks of class.

Academic Honesty:

Students should demonstrate academic honesty by doing original work and by giving appropriate credit to the ideas of others. Academic dishonesty is the act of presenting information, ideas, and/or concepts as one's own when in reality they are the results of another person's creativity and effort. A faculty member who believes a situation involving academic dishonesty has been detected may assign a failing grade for that assignment or examination, or, depending on the seriousness of the offense, for the course. Faculty should follow and students may appeal using the procedure in the university Catalog.

See http://catalog.pointloma.edu/content.php?catoid=24&navoid=1581#Academic_Honesty for definitions of kinds of academic dishonesty and for further policy information.

Final Exam: Date and Time:

The final exam date and time is set by the university at the beginning of the semester and may not be changed by the instructor. This schedule can be found on the university website and in the course calendar. No requests for early examinations will be approved. Only in the case that a student is required to take three exams during the same day of finals week, is an instructor authorized to consider changing the exam date and time for that particular student.

Copyright Protected Materials:

Point Loma Nazarene University, as a non-profit educational institution, is entitled by law to use materials protected by the US Copyright Act for classroom education. Any use of those materials outside the class may violate the law.

Anticipated Schedule

Mon	Tues	Wed	Thurs	Fri
Aug 29 (on Tuesday) Syllabus, 1.1-1.5	30 No lab	31 A1, 2.1-2.3 Intro Assembly	Sept 1	2 2.4, Hex, A9 (SPIM)
5 Labor Day	6 MIPS lab 1	7 2.5 instr formats, Arith, load, store	8	9 2.6, 2.7 Logic, conditional
12 HW quiz A2-A5 assemblers	13 MIPS lab 2	14 A6-A10, 2.8 and 2.9, I/O and procedure calls	15	16 2.9-2.10 Addressing modes
19 HW quiz 2.16, 2.17 real stuff	20 MIPS lab 3	21 1.6-1.10 performance and power	22	23 Exercises and Review
26 Start circuits	27 Exam 1 7:45	28 K maps B1, B2	29	30 More K maps , exercises
Oct 3 HW quiz 3.1-3.3 arithmetic op	4 Logisim lab 1	5 More 3.3 and 3.6 (FP)	6	7 3.7-3.8 subword parallelism
10 B3, B4 multiplexors & decoders, VHDL	11 Logisim 2	12 HW Quiz Start basic ALU - B5,B6	13	14 More basic ALU
17 Design ALU for lab	18 ALU lab	19 B7, B8 Flipflops	20	21 Fall break
24 4.1-4.3 Rtype and Mem instructions	25 More ALU lab	26 HW Quiz 4.3, 4.4 Branches, Control	27	28 4.5 Intro pipelining
31 4.6 pipelining	Nov 1 Pipelining exercises	2 4.7 Data Hazards	3	4 4.8 Control Hazards
7 4.10, 4.12 ILP	8 TBD	9 HW quiz Review	10	11 Exam 2
14 5.1-5.3 Mem basics	15 Exam review	16 5.4 cache performance	17	18 More cache
21 HW quiz, intro lab	22 Cache lab	23 Thanksgiving	24 TG	25 TG
28 5.7-5.8 virtual mem	29 Cache lab	30 5.10 Parallelism and cache coherence	Dec 1	2 HW quiz 6.1-6.3 architectures
5 6.4 - 6.5 More parallel	6 Demo cache labs	7 More parallel	8	9 Look at HW, review
12 Final 7:30	13	14	15	16